

### In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1        1.     (Original) A shift overflow detection circuit for a  
2 shifter having a data bit length of M and a shift control value bit  
3 length of N comprising:

4        a plurality of circuit elements disposed in M rows and N  
5 columns, each circuit element(i,d) of the i-th row and the d-th  
6 column having two inputs and an output, a circuit element of a last  
7 column generating an output of said shift overflow detection  
8 circuit, wherein:

9            if  $d=2^n*2^i$  where n is in the range  $1 \leq n \leq ((M/2^{i+1})-1)$ ,  
10 then element(i,d) is an OR gate having a first input connected  
11 to said output of element(i-1,d+2<sup>i</sup>) and a second input  
12 connected to said output of element(i-1,d),

13           if  $d=2^n*2^i+2^j$  where n is in the range  $1 \leq n \leq ((M/2^{i+1})-1)$   
14 and j is in the range  $0 \leq j \leq i-1$ , then element(i,d) is a  
15 multiplexer having a first input connected to said output of  
16 element(i-1,d), a second input connected to said output of  
17 element(i-1,d+2<sup>i</sup>) and a control input receiving the i-bit of  
18 said shift control value,

19           if  $d=(2^n+1)*2^i$ , where n is in the range  $1 \leq n \leq ((M/2^{i+1})-$   
20 1) and j is in the range  $0 \leq j \leq i-1$ , then element(i,d) is a  
21 multiplexer having a first input connected to said output of  
22 element(i-1,d), a second input receiving 0 and a control input  
23 receiving the i-bit of said shift control value, and

24           for all other combinations of i and d, there is no  
25 element(i,d).

1        2.     (Original) The shift overflow detector of claim 1,  
2 wherein:

3 each multiplexer includes

4 a first pass gate having a input connected to said first  
5 input of said multiplexer, an output connected to said output  
6 of said multiplexer and receiving said control input in a  
7 first polarity whereby said first pass gate is conducting when  
8 said control input is 1, and

9 a second pass gate having a input connected to said  
10 second input of said multiplexer, an output connected to said  
11 output of said multiplexer and receiving said control input in  
12 a second polarity opposite to said first polarity whereby said  
13 first pass gate is conducting when said control input is 0.

1 3. (Currently Amended) A shift overflow detection circuit  
2 having a 16 bit data length [D15:D0] and a shift control value of 4  
3 bits [S3:S0], comprising:

4 a first multiplexer having a first input receiving data bit  
5 D1, a second input receiving 0, a control input receiving shift  
6 value bit S0 and an output;

7 a first OR gate having a first input receiving data bit D2, a  
8 second input receiving data bit D3 and an output;

9 a second multiplexer having a first input receiving data bit  
10 D3, a second input receiving 0, a control input receiving shift  
11 value bit S0 and an output;

12 a second OR gate having a first input receiving data bit D4, a  
13 second input receiving data bit D5 and an output;

14 a third multiplexer having a first input receiving data bit  
15 D5, a second input receiving 0, a control input receiving shift  
16 value bit S0 and an output;

17 a third OR gate having a first input receiving data bit D6, a  
18 second input receiving data bit D7 and an output;

19 a fourth multiplexer having a first input receiving data bit  
20 D7, a second input receiving 0, a control input receiving shift  
21 value bit S0 and an output;  
22 a fourth OR gate having a first input receiving data bit D8, a  
23 second input receiving data bit D9 and an output;  
24 a fifth multiplexer having a first input receiving data bit  
25 D9, a second input receiving 0, a control input receiving shift  
26 value bit S0 and an output;  
27 a fifth OR gate having a first input receiving data bit D10, a  
28 second input receiving data bit D11 and an output;  
29 a sixth multiplexer having a first input receiving data bit  
30 D11, a second input receiving 0, a control input receiving shift  
31 value bit S0 and an output;  
32 a sixth OR gate having a first input receiving data bit D12, a  
33 second input receiving data bit D13 and an output;  
34 a seventh multiplexer having a first input receiving data bit  
35 D13, a second input receiving 0, a control input receiving shift  
36 value bit S0 and an output;  
37 a seventh OR gate having a first input receiving data bit D14,  
38 a second input receiving data bit D15 and an output;  
39 an eighth multiplexer having a first input receiving data bit  
40 D15, a second input receiving 0, a control input receiving shift  
41 value bit S0 and an output;  
42 a ninth multiplexer having a first input connected to said  
43 output of said first multiplexer, a second input connected to said  
44 output of said second multiplexer, a control input receiving shift  
45 control value bit S1 and an output;  
46 a tenth multiplexer having a first input connected to said  
47 output of said first OR gate, a second input receiving 0, a control  
48 input receiving shift control value bit S1 and an output;

49 an eighth OR gate having a first input connected to said  
50 output of said second OR gate, a second ~~output~~ input connected to  
51 said output of said third OR gate and an output;  
52 an eleventh multiplexer having a first input connected to said  
53 output of said third multiplexer, a second input connected to said  
54 output of said fourth multiplexer, a control input receiving shift  
55 control value bit S1 and an output;  
56 a twelfth multiplexer having a first input connected to said  
57 output of said third OR gate, a second input receiving 0, a control  
58 input receiving shift control value bit S1 and an output;  
59 a ninth OR gate having a first input connected to said output  
60 of said fourth OR gate, a second output connected to said output of  
61 said fifth OR gate and an output;  
62 a thirteenth multiplexer having a first input connected to  
63 said output of said fifth multiplexer, a second input connected to  
64 said output of said sixth multiplexer, a control input receiving  
65 shift control value bit S1 and an output;  
66 a fourteenth multiplexer having a first input connected to  
67 said output of said fifth OR gate, a second input receiving 0, a  
68 control input receiving shift control value bit S1 and an output;  
69 a tenth OR gate having a first input connected to said output  
70 of said sixth OR gate, a second output connected to said output of  
71 said seventh OR gate and an output;  
72 a fifteenth multiplexer having a first input connected to said  
73 output of said seventh multiplexer, a second input connected to  
74 said output of said eighth multiplexer, a control input receiving  
75 shift control value bit S1 and an output;  
76 a sixteenth multiplexer having a first input connected to said  
77 output of said seventh OR gate, a second input receiving 0, a  
78 control input receiving shift control value bit S1 and an output;  
79 a seventeenth multiplexer having a first input connected to  
80 said output of said ninth multiplexer, a second input connected to

81 said output of said eleventh multiplexer, a control input receiving  
82 shift control value bit S2 and an output;  
83 an eighteenth multiplexer having a first input connected to  
84 said output of said tenth multiplexer, a second input connected to  
85 said output of said twelfth multiplexer, a control input receiving  
86 shift control value bit S2 and an output;  
87 a nineteenth multiplexer having a first input connected to  
88 said output of said eighth OR gate, a second input receiving 0, a  
89 control input receiving shift control value bit S2 and an output;  
90 an eleventh OR gate having a first input connected to said  
91 output of said ninth OR gate, a second output connected to said  
92 output of said tenth OR gate and an output;  
93 a twentieth multiplexer having a first input connected to said  
94 output of said thirteenth multiplexer, a second input connected to  
95 said output of said fifteenth multiplexer, a control input  
96 receiving shift control value bit S2 and an output;  
97 a twenty first multiplexer having a first input connected to  
98 said output of said fourteenth multiplexer, a second input  
99 connected to said output of said sixteenth multiplexer, a control  
100 input receiving shift control value bit S2 and an output;  
101 a twenty second multiplexer having a first input connected to  
102 said output of said tenth OR gate, a second input receiving 0, a  
103 control input receiving shift control value bit S2 and an output;  
104 a twenty third multiplexer having a first input connected to  
105 said output of said seventeenth multiplexer, a second input  
106 connected to said output of said twentieth multiplexer, a control  
107 input receiving shift control value bit S3 and an output;  
108 a twenty fourth multiplexer having a first input connected to  
109 said output of said eighteenth multiplexer, a second input  
110 connected to said output of said twenty first multiplexer, a  
111 control input receiving shift control value bit S3 and an output;

112 a twenty fifth multiplexer having a first input connected to  
113 said output of said nineteenth multiplexer, a second input  
114 connected to said output of said twenty second multiplexer, a  
115 control input receiving shift control value bit S3 and an output;  
116 a twenty sixth multiplexer having a first input connected to  
117 said output of said eleventh OR gate, a second input receiving 0, a  
118 control input receiving shift control value bit S3 and an output;  
119 a twelfth OR gate having a first input connected to said  
120 output of said twenty third multiplexer, a second input connected  
121 to said output of said twenty fourth multiplexer and an output;  
122 a thirteenth OR gate having a first input connected to said  
123 output of said twenty fifth multiplexer, a second input connected  
124 to said output of said twenty sixth multiplexer and an output; and  
125 a fourteenth OR gate having a first input connected to said  
126 output of said twelfth OR gate, a second input connected to said  
127 output of said thirteenth OR gate and an output forming an output  
128 of said shift overflow detection circuit.

1 4. (Currently Amended) The shift overflow detector of claim  
2 2, wherein:  
3 each of said first ~~to~~ multiplexer, said second multiplexer,  
4 said third multiplexer, said fourth multiplexer, said fifth  
5 multiplexer, said sixth multiplexer, said seventh multiplexer, said  
6 eighth multiplexer, said ninth multiplexer, said tenth multiplexer,  
7 said eleventh multiplexer, said twelfth multiplexer, said  
8 thirteenth multiplexer, said fourteenth multiplexer, said fifteenth  
9 multiplexer, said sixteenth multiplexer, said seventh multiplexer,  
10 said eighteenth multiplexer, said nineteenth multiplexer, said  
11 twentieth multiplexer, said twenty first multiplexer, said twenty  
12 second multiplexer, said twenty third multiplexer, said twenty  
13 fourth multiplexer, said twenty fifth multiplexer and said twenty  
14 sixth multiplexer includes

15           a first pass gate having a input connected to said first  
16       input of said multiplexer, an output connected to said output  
17       of said multiplexer and receiving said control input in a  
18       first polarity whereby said first pass gate is conducting when  
19       said control input is 1, and  
20           a second pass gate having a input connected to said  
21       second input of said multiplexer, an output connected to said  
22       output of said multiplexer and receiving said control input in  
23       a second polarity opposite to said first polarity whereby said  
24       first pass gate is conducting when said control input is 0.

1       5.   (Currently Amended) A shift overflow detection circuit  
2       having a 32 bit data length [D31:D0] and a shift control value of 5  
3       bits [S4:S0], comprising:  
4           a first multiplexer having a first input receiving data bit  
5       D1, a second input receiving data bit D3, a control input receiving  
6       shift control value bit S1 and an output;  
7           a first NAND gate having a first input connected to said  
8       output of said first multiplexer, a second input receiving shift  
9       control value bit S0 and an output;  
10          a first OR gate having a first input receiving data bit D2, a  
11       second input receiving data bit D3 and an output;  
12          a second NAND gate having a first input connected to said  
13       output of said first OR gate, a second input receiving shift  
14       control value bit S0 and an output;  
15          a first NOR gate having a first input receiving data bit D4, a  
16       second input receiving data bit D5 and an output;  
17          a second multiplexer having a first input receiving data bit  
18       D5, a second input receiving data bit D7, a control input receiving  
19       shift control value bit S1 and an output;

20           a third NAND gate having a first input connected to said  
21 output of said second multiplexer, a second input receiving shift  
22 control value bit S0 and an output;  
23           a second NOR gate having a first input receiving data bit D6,  
24 a second input receiving data bit D7 and an output;  
25           a second OR gate having a first input receiving data bit D6, a  
26 second input receiving data bit D7 and an output;  
27           a fourth NAND gate having a first input connected to said  
28 output of said second OR gate, a second input receiving shift  
29 control value bit S0 and an output;  
30           a third NOR gate having a first input receiving data bit D8, a  
31 second input receiving data bit D9 and an output;  
32           a third multiplexer having a first input receiving data bit  
33 D9, a second input receiving data bit D11, a control input  
34 receiving shift control value bit S1 and an output;  
35           a fifth NAND gate having a first input connected to said  
36 output of said third multiplexer, a second input receiving shift  
37 control value bit S0 and an output;  
38           a fourth NOR gate having a first input receiving data bit D10,  
39 a second input receiving data bit D11 and an output;  
40           a third OR gate having a first input receiving data bit D10, a  
41 second input receiving data bit D11 and an output;  
42           a sixth NAND gate having a first input connected to said  
43 output of said third OR gate, a second input receiving shift  
44 control value bit S0 and an output;  
45           a fifth NOR gate having a first input receiving data bit D12,  
46 a second input receiving data bit D13 and an output;  
47           a fourth multiplexer having a first input receiving data bit  
48 D13, a second input receiving data bit D15, a control input  
49 receiving shift control value bit S1 and an output;



50 a seventh NAND gate having a first input connected to said  
51 output of said fourth multiplexer, a second input receiving shift  
52 control value bit S0 and an output;  
53 a sixth NOR gate having a first input receiving data bit D14,  
54 a second input receiving data bit D15 and an output;  
55 a fourth OR gate having a first input receiving data bit D14,  
56 a second input receiving data bit D15 and an output;  
57 an eighth NAND gate having a first input connected to said  
58 output of said fourth OR gate, a second input receiving shift  
59 control value bit S0 and an output;  
60 a seventh NOR gate having a first input receiving data bit  
61 D16, a second input receiving data bit D17 and an output;  
62 a fifth multiplexer having a first input receiving data bit  
63 D17, a second input receiving data bit D19, a control input  
64 receiving shift control value bit S1 and an output;  
65 a ninth NAND gate having a first input connected to said  
66 output of said fifth multiplexer, a second input receiving shift  
67 control value bit S0 and an output;  
68 an eighth NOR gate having a first input receiving data bit  
69 D18, a second input receiving data bit D19 and an output;  
70 a fifth OR gate having a first input receiving data bit D18, a  
71 second input receiving data bit D19 and an output;  
72 a tenth NAND gate having a first input connected to said  
73 output of said fifth OR gate, a second input receiving shift  
74 control value bit S0 and an output;  
75 a ninth NOR gate having a first input receiving data bit D20,  
76 a second input receiving data bit D21 and an output;  
77 a sixth multiplexer having a first input receiving data bit  
78 D21, a second input receiving data bit D23, a control input  
79 receiving shift control value bit S1 and an output;

80 an eleventh NAND gate having a first input connected to said  
81 output of said sixth multiplexer, a second input receiving shift  
82 control value bit S0 and an output;  
83 a tenth NOR gate having a first input receiving data bit D22,  
84 a second input receiving data bit D23 and an output;  
85 a sixth OR gate having a first input receiving data bit D22, a  
86 second input receiving data bit D23 and an output;  
87 a twelfth NAND gate having a first input connected to said  
88 output of said sixth OR gate, a second input receiving shift  
89 control value bit S0 and an output;  
90 an eleventh NOR gate having a first input receiving data bit  
91 D24, a second input receiving data bit D25 and an output;  
92 a seventh multiplexer having a first input receiving data bit  
93 D25, a second input receiving data bit D27, a control input  
94 receiving shift control value bit S1 and an output;  
95 a thirteenth NAND gate having a first input connected to said  
96 output of said seventh multiplexer, a second input receiving shift  
97 control value bit S0 and an output;  
98 a twelfth NOR gate having a first input receiving data bit  
99 D26, a second input receiving data bit D27 and an output;  
100 a seventh OR gate having a first input receiving data bit D26,  
101 a second input receiving data bit D27 and an output;  
102 a fourteenth NAND gate having a first input connected to said  
103 output of said seventh OR gate, a second input receiving shift  
104 control value bit S0 and an output;  
105 a thirteenth NOR gate having a first input receiving data bit  
106 D28, a second input receiving data bit D29 and an output;  
107 an eighth multiplexer having a first input receiving data bit  
108 D29, a second input receiving data bit D31, a control input  
109 receiving shift control value bit S1 and an output;

110           a fifteenth NAND gate having a first input connected to said  
111 output of said eighth multiplexer, a second input receiving shift  
112 control value bit S0 and an output;  
113           a fourteenth NOR gate having a first input receiving data bit  
114 D30, a second input receiving data bit D31 and an output;  
115           an eighth OR gate having a first input receiving data bit D30,  
116 a second input receiving data bit D31 and an output;  
117           a sixteenth NAND gate having a first input connected to said  
118 output of said eighth OR gate, a second input receiving shift  
119 control value bit S0 and an output;  
120           a seventeenth NAND gate having a first input connected to said  
121 output of said first NAND gate, a second input connected to said  
122 output of said second NAND gate, a third input connected to said  
123 output of said first NOR gate, a fourth input connected to said  
124 output of said second NOR gate and an output;  
125           an eighteenth NAND gate having a first input connected to said  
126 output of said third NAND gate, a second input connected to said  
127 output of said fourth NAND gate and an output;  
128           a nineteenth NAND gate having a first input connected to said  
129 output of said third NOR gate, a second input connected to said  
130 output of said fourth NOR gate, a third input connected to said  
131 output of said fifth NOR gate, a fourth input connected to said  
132 output of said sixth NOR gate and an output;  
133           a twentieth NAND gate having a first input connected to said  
134 output of said fifth NAND gate, a second input connected to said  
135 output of said sixth NAND gate, a third input connected to said  
136 output of said fifth NOR gate, a fourth input connected to said  
137 output of said sixth NOR gate and an output;  
138           a twenty first NAND gate having a first input connected to  
139 said output of said seventh NAND gate, a second input connected to  
140 said output of said eighth NAND gate and an output;

141       a twenty second NAND gate having a first input connected to  
142 said output of said seventh NOR gate, a second input connected to  
143 said output of said eighth NOR gate, a third input connected to  
144 said output of said ninth NOR gate, a fourth input connected to  
145 said output of said tenth NOR gate and an output;  
146       a twenty third NAND gate having a first input connected to  
147 said output of said ninth NAND gate, a second input connected to  
148 said output of said tenth NAND gate, a third input connected to  
149 said output of said ninth NOR gate, a fourth input connected to  
150 said output of said tenth NOR gate and an output;  
151       a twenty fourth NAND gate having a first input connected to  
152 said output of said eleventh NAND gate, a second input connected to  
153 said output of said twelfth NAND gate and an output;  
154       a twenty fifth NAND gate having a first input connected to  
155 said output of said eleventh NOR gate, a second input connected to  
156 said output of said twelfth NOR gate, a third input connected to  
157 said output of said thirteenth NOR gate, a fourth input connected  
158 to said output of said fourteenth NOR gate and an output;  
159       a twenty sixth NAND gate having a first input connected to  
160 said output of said thirteenth NAND gate, a second input connected  
161 to said output of said fourteenth NAND gate, a third input  
162 connected to said output of said thirteenth NOR gate, a fourth  
163 input connected to said output of said fourteenth NOR gate and an  
164 output;  
165       a twenty seventh NAND gate having a first input connected to  
166 said output of said fifteenth NAND gate, a second input connected  
167 to said output of said sixteenth NAND gate and an output;  
168       a seventeenth multiplexer having a first input connected to  
169 said output of said nineteenth NAND gate, a second input connected  
170 to said twenty fifth NAND gate, a control input receiving shift  
171 control value bit S4 and an output;

172 a twenty eighth NAND gate having a first input connected to  
173 said output of said seventeenth multiplexer, a second input  
174 receiving shift control value bit S3 and an output;  
175 a ninth OR gate having a first input connected to said output  
176 of said twenty second NAND gate, a second input connected to said  
177 output of said twenty fifth NAND gate and an output;  
178 a twenty ninth NAND gate having a first input connected to  
179 said output of said ninth OR gate, a second input receiving shift  
180 control value bit S4 and an output;  
181 an inverting multiplexer having a first input connected to  
182 said output of said seventeenth NAND gate, a second input connected  
183 to said output of said eighteenth NAND gate, a third input  
184 connected to said output of said twentieth NAND gate, a fourth  
185 input connected to said output of said twenty first NAND gate, a  
186 fifth input connected to said output of said twenty third NAND  
187 gate, a sixth input connected to said output of said twenty fourth  
188 NAND gate, a seventh input connected to said output of said twenty  
189 sixth NAND gate, an eighth input connected to said output of said  
190 twenty seventh NAND gate, three control ~~input~~ inputs receiving  
191 respective shift control value bits S4, S3 and S2 and an output,  
192 whereby said inverting multiplexer outputs a inverted first input  
193 if said shift control bits S4, S3 and S2 are "111", a inverted  
194 second input if said shift control bits S4, S3 and S2 are "110", a  
195 inverted third input if said shift control bits S4, S3 and S2 are  
196 "101", a inverted fourth input if said shift control bits S4, S3  
197 and S2 are "100", a inverted fifth input if said shift control bits  
198 S4, S3 and S2 are "011", a inverted sixth input if said shift  
199 control bits S4, S3 and S2 are "010", a inverted seventh input if  
200 said shift control bits S4, S3 and S2 are "001" and a inverted  
201 eighth input if said shift control bits S4, S3 and S2 are "000";  
202 and

203 a thirtieth NAND gate having a first input connected to said  
204 output of said inverting multiplexer, a second input connected to  
205 said output of said twenty eighth NAND gate, a third input  
206 connected to said output of said twenty ninth NAND gate and an  
207 output forming an output of said shift overflow detection circuit.

1 6. (Original) The shift overflow detector of claim 5, wherein:  
2 each of said first to seventeenth multiplexer includes  
3 a first pass gate having a input connected to said first  
4 input of said multiplexer, an output connected to said output  
5 of said multiplexer and receiving said control input in a  
6 first polarity whereby said first pass gate is conducting when  
7 said control input is 1, and  
8 a second pass gate having a input connected to said  
9 second input of said multiplexer, an output connected to said  
10 output of said multiplexer and receiving said control input in  
11 a second polarity opposite to said first polarity whereby said  
12 first pass gate is conducting when said control input is 0.

1 7. (Original) The shift overflow detector of claim 5, wherein:  
2 said inverting multiplexer includes  
3 a first inverter having a input receiving shift control  
4 value bit S2 and an output,  
5 a second inverter having a input receiving shift control  
6 value bit S3 and an output,  
7 a third inverter having a input receiving shift control  
8 value bit S4 and an output,  
9 a first NAND gate having a first input receiving shift  
10 control value S2, a second input receiving shift control value  
11 S3, a third input receiving shift control value S4 and an  
12 output,

13           a second NAND gate having a first input connected to said  
14           output of said first inverter, a second input receiving shift  
15           control value S3, a third input receiving shift control value  
16           S4 and an output,

17           a third NAND gate having a first input receiving shift  
18           control value S2, a second input connected to said output of  
19           said second inverter, a third input receiving shift control  
20           value S4 and an output,

21           a fourth NAND gate having a first input connected to said  
22           output of said first inverter, a second input connected to  
23           said output of said second inverter, a third input receiving  
24           shift control value S4 and an output,

25           a fifth NAND gate having a first input receiving shift  
26           control value S2, a second input receiving shift control value  
27           S3, a third input connected to said output of said third  
28           inverter and an output,

29           a sixth NAND gate having a first input connected to said  
30           output of said first inverter, a second input receiving shift  
31           control value S3, a third input connected to said output of  
32           said third inverter and an output,

33           a seventh NAND gate having a first input receiving shift  
34           control value S2, a second input connected to said output of  
35           said second inverter, a third input connected to said output  
36           of said third inverter and an output,

37           a eighth NAND gate having a first input connected to said  
38           output of said first inverter, a second input connected to  
39           said output of said second inverter, a third input connected  
40           to said output of said third inverter and an output,

41           a fourth inverter having an input connected to said  
42           output of said first NAND gate and an output,

43           a fifth inverter having an input connected to said output  
44           of said second NAND gate and an output,

45           a sixth inverter having an input connected to said output  
46 of said third NAND gate and an output,

47           a seventh inverter having an input connected to said  
48 output of said fourth NAND gate and an output,

49           a eighth inverter having an input connected to said  
50 output of said fifth NAND gate and an output,

51           a ninth inverter having an input connected to said output  
52 of said sixth NAND gate and an output,

53           a tenth inverter having an input connected to said output  
54 of said seventh NAND gate and an output,

55           a eleventh inverter having an input connected to said  
56 output of said eighth NAND gate and an output,

57           a first pass gate having an input connected to said first  
58 input of said inverting multiplexer, a first control input  
59 connected to said output of said first NAND gate, a second  
60 control input connected to said output of said fourth inverter  
61 and an output,

62           a second pass gate having an input connected to said  
63 second input of said inverting multiplexer, a first control  
64 input connected to said output of said second NAND gate, a  
65 second control input connected to said output of said fifth  
66 inverter and an output,

67           a third pass gate having an input connected to said third  
68 input of said inverting multiplexer, a first control input  
69 connected to said output of said third NAND gate, a second  
70 control input connected to said output of said sixth inverter  
71 and an output,

72           a fourth pass gate having an input connected to said  
73 fourth input of said inverting multiplexer, a first control  
74 input connected to said output of said fourth NAND gate, a  
75 second control input connected to said output of said seventh  
76 inverter and an output,



77           a fifth pass gate having an input connected to said fifth  
78       input of said inverting multiplexer, a first control input  
79       connected to said output of said fifth NAND gate, a second  
80       control input connected to said output of said eighth inverter  
81       and an output,  
82           a sixth pass gate having an input connected to said sixth  
83       input of said inverting multiplexer, a first control input  
84       connected to said output of said sixth NAND gate, a second  
85       control input connected to said output of said ninth inverter  
86       and an output,  
87           a seventh pass gate having an input connected to said  
88       seventh input of said inverting multiplexer, a first control  
89       input connected to said output of said seventh NAND gate, a  
90       second control input connected to said output of said tenth  
91       inverter and an output,  
92           an eighth pass gate having an input connected to said  
93       eighth input of said inverting multiplexer, a first control  
94       input connected to said output of said eighth NAND gate, a  
95       second control input connected to said output of said eleventh  
96       inverter and an output, and  
97           a twelfth inverter having an input connected to said  
98       output of said first, second, third, fourth, fifth, sixth,  
99       seventh and eighth pass gates and an output forming said  
100      output of said inverting multiplexer.